International Journal of Thermal Sciences 48 (2009) 1416–1422

Contents lists available at ScienceDirect

International Journal of Thermal Sciences

www.elsevier.com/locate/ijts

Subcooled flow boiling heat transfer of FC-72 from silicon chips fabricated with micro-pin-fins

Minzhe Yuan, Jinjia Wei *, Yanfang Xue, Jiabin Fang

State Key Laboratory of Multiphase Flow in Power Engineering, Xi'an Jiaotong University, Xi'an 710049, China

ARTICLE INFO

Article history:
Received 11 August 2008
Received in revised form 25 November 2008
Accepted 25 November 2008
Available online 17 December 2008

Keywords:
Flow boiling
Heat transfer
High heat flux
Micro-pin-fin
FC-72

ABSTRACT

Experiments were conducted to study the subcooled flow boiling heat transfer performance of FC-72 over silicon chips. For boiling heat transfer enhancement, two kinds of micro-pin-fins having fin thickness of 50 μm and fin heights of 60 and 120 μm, respectively, were fabricated on the silicon chip surface with the dry etching technique. The fin pitch was twice the fin thickness. The experiments were conducted at the fluid velocities of 0.5, 1 and 2 m/s and the liquid subcoolings of 15, 25 and 35 K. The micro-pin-finned surfaces showed a sharp increase in heat flux with increasing wall superheat and a large heat transfer enhancement compared to a smooth surface. The nucleate flow boiling curves for the two micro-pin-finned surfaces collapsed to one line showing insensitivity to fluid velocity and subcooling, while the critical heat flux values increased with fluid velocity and subcooling. The micro-pin-finned surface with a larger fin height of 120 μm provided a better flow boiling heat transfer performance and a maximum critical heat flux of 145 W/cm^2. The wall temperature at the critical heat flux for the micro-pin-finned surfaces was less than 85 °C for the reliable operation of LSI chips.

1. Introduction

Sophisticated cooling technology is required for the high-heat-emission electronic components to maintain relatively constant component temperature below the junction temperature, approximately 85 °C for most mainframe memory and logic chips. Direct liquid cooling, involving boiling heat transfer, by use of dielectric fluids has been considered as one of the promising cooling schemes. Primary issues related to the direct liquid cooling of microelectronic components are mitigation of the incipience temperature overshoot, enhancement of established nucleate boiling and elevation of critical heat flux (CHF).

Treated surfaces have been found to have great potential in enhancing boiling heat transfer from electronics, significantly reducing chip surface temperature and increasing CHF. Enhancement studies have commonly considered randomly roughened surfaces [1,2], surfaces with regularly spaced artificial nucleation sites (cavities and low-profiles) [2–5] and porous surfaces [6,7]. The nucleate boiling curves of most of these treated surfaces experienced two distinct regions. In the lower nucleate boiling region, isolate bubble grew and departed from the heater surface and boiling curves had a larger slope, whereas in the higher boiling region, the discrete bubbles began to coalesce and bubble coalescence increased with increasing heat flux to finally form large vapor mushrooms hovering above the heated surface, which made the access of fresh bulk liquid into the heat surface difficult, resulting in a noticeably decreased slope in boiling curves. The enhancement of CHF often leads to a high chip surface temperature greater than 85 °C, the junction temperature of electronic elements.

Recently, Honda and Wei [8–11] made a noticeable progress in nucleate boiling enhancement by use of micro-pin-fins (10–50 μm in thickness and 60–200 μm in height) which were fabricated by the dry etching technique. From the boiling incipience to the critical heat flux, the temperature of the micro-pin-finned surfaces almost did not increase with the heat flux. The increase of CHF could reach more than twice that of a smooth chip and the wall temperature at the CHF point was lower than 85 °C. Therefore, the micro-pin-fined surface with the fin thickness of 10–50 μm appears to be one promising enhanced surface for efficient electronic components cooling schemes. However, the micro-pin-finned surface was only tested in a pool of FC-72, and its enhancement ability under flow boiling is not yet revealed. Lie et al. [12] studied the saturated flow boiling heat transfer of FC-72 on a heated pin-finned silicon chip with large fin thicknesses of 100 and 200 μm. They only investigated the boiling heat transfer at a low heat flux region ($q < 10$ W/cm^2). For cooling high-heat-flux chips, the boiling heat transfer performance at a high heat flux region up to CHF should be clarified. In addition, Honda and Wei [8–11] showed that the pool boiling heat transfer performance for their micro-pin-finned surfaces is much better than the pin-finned surface with the fin thickness of about 300 μm used by Anderson and Mudawar [2]. Therefore, it is expected that the micro-pin-finned chips with the

* Corresponding author.
E-mail address: jjwei@mail.xjtu.edu.cn (J. Wei).

1290-0729/$ – see front matter
doi:10.1016/j.ijthermalsci.2008.11.018

Nomenclature

A	surface area of chip ..... cm^2	T_w	wall temperature ..... °C
h	fin height ..... μm	t	fin thickness ..... μm
p	fin pitch ..... μm	V	fluid velocity ..... m/s
q	heat flux ..... W/cm^2	ΔT_b	wall superheat $= T_w - T_b$ ..... K
q_{CHF}	critical heat flux ..... W/cm^2	ΔT_{sat}	wall superheat $= T_w - T_{sat}$ ..... K
T_b	temperature of bulk liquid ..... °C	ΔT_{sub}	liquid subcooling $= T_{sat} - T_b$ ..... K
T_{sat}	saturation temperature ..... °C		

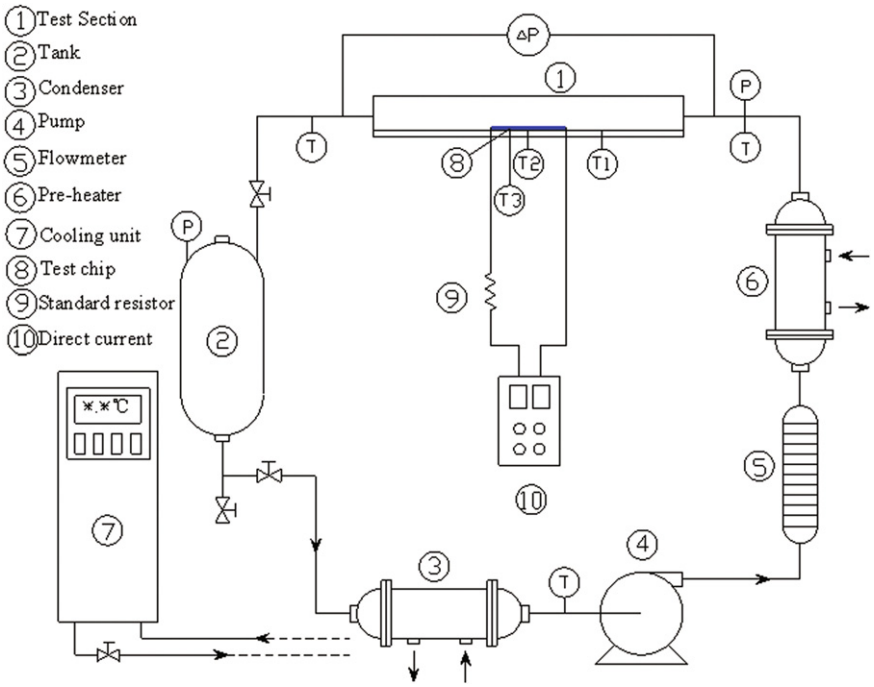


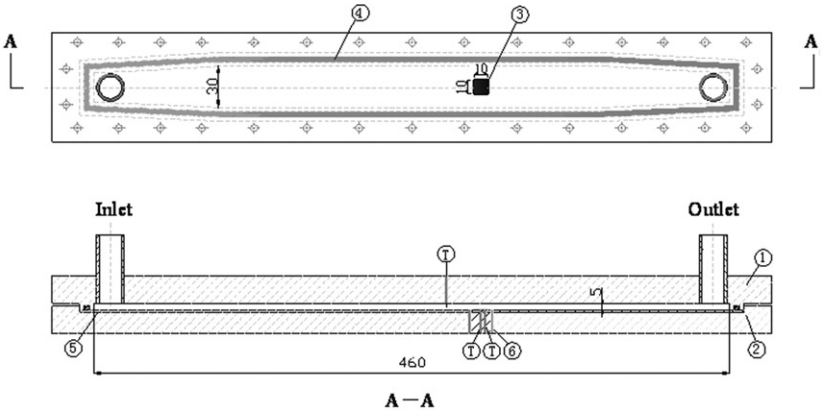
Fig. 1. Flow boiling test loop.

fin thickness of 10–50 μm should differ from those of Lie et al. [12], and their flow boiling heat transfer performance up to the CHF is worthy of studying. Some researchers such as Mudawar and Maddox [13], Kutateladze and Burakov [14], Samant and Simon [15], and Rainey and You [16], have found that both of fluid velocity and subcooling had significant positive effects on the nucleate boiling curve and the critical heat flux of their thin film heater. Therefore, the objective of this paper is to study the combined effects of fluid velocity and subcooling on the flow boiling heat transfer of FC-72 over micro-pin-fined surfaces for further enhancement of boiling heat transfer to cool high-heat-flux electronic devices. Two micro-pin-finned chips having the same fin thickness of 50 μm and different fin heights of 60 (chip PF50-60) and 120 μm (chip PF50-120), respectively, were tested. A smooth chip was also tested for comparison. The flow boiling data were also compared with the previous published pool boiling data for the same micro-pin-finned surfaces.

2. Experimental apparatus and procedure

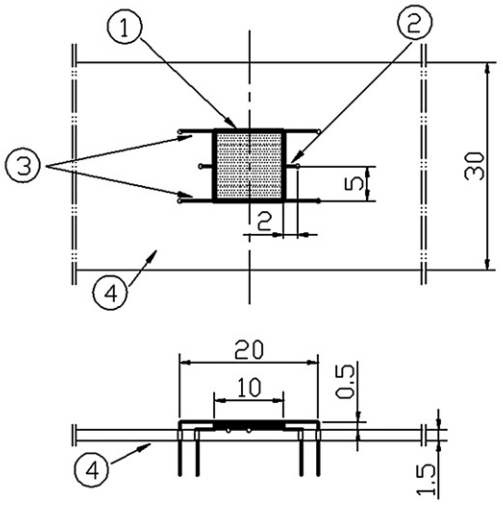
The flow boiling test facility used for the present study is shown schematically in Fig. 1. It is a closed-loop circuit consisting of a tank, a scroll pump, a test section, two heat exchangers and a turbine flowmeter. The tank serves as a fluid reservoir and pressure regulator during testing. The condenser prior to the pump is used to cool the fluid and prevent cavitation in the pump. The pre-heater prior to the test section is used to control the test section inlet temperature. The pump combined with a converter to control the mass flow rate. To ensure proper inlet pressure control, a pressure transducer was installed at the inlet of the test section. The pressure drop across the test section was also measured by a pressure difference transducer. The flowmeter and the sensors for pressure and pressure difference have the function of outputting 4–20 mA current signals and were measured directly by a data acquisition system.

The test chip is a P-doped N-type square silicon chip with a side length of 10 mm and a thickness of 0.5 mm. The chip was provided from Yamanaka Semiconductor Corporation, Japan. P was doped by using high temperature diffusion method with a temperature range of 800–1400 °C. The doping depth is in the range of 0.2–10 μm. The electrical resistance of the 1 cm^2 square smooth silicon chip is about 50 Ohm. The chip is bonded on a substrate made of polycarbonate using epoxy adhesive, and fixed in the horizontal, upward facing orientation on the bottom surface of a 5 mm high and 30 mm wide horizontal channel as shown in Fig. 2. The chip was located 300 mm (60 hydraulic dia.) from the test section inlet so that the fluid flow at it is estimated to be fully developed turbulent flow for the present fluid velocity range. The side surfaces of the chip were covered with adhesive to minimize heat loss. Therefore, only the upper surface of the chip was effective for heat transfer. The chip was Joule heated by using a d.c. power supply. The power supply was connected to a standard resistor (1 Ω) and the test chip. The standard resistor was used to measure the electric current in the circuit. Two 0.25 mm diameter copper wires



1 upper cover 2 lower cover 3 test chip 4 O-ring 5 polycarbonate plate

(a) Test section



1 test chip 2 thermocouples 3 copper lead wires 4 polycarbonate plate

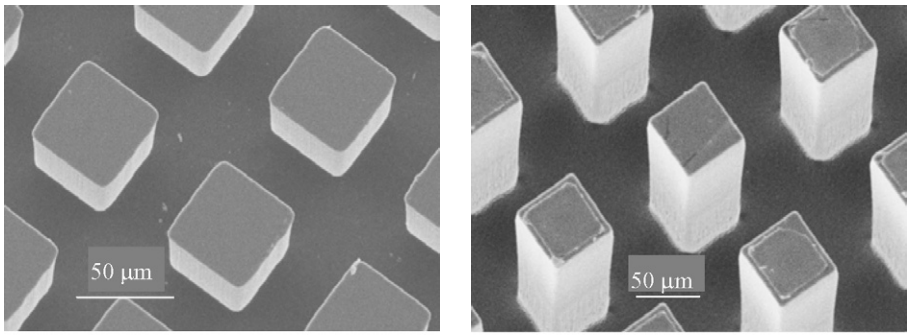
(b) Details of heater assembly

Fig. 2. Schematic diagrams of test section and heater assembly. (a) Test section. (b) Details of heater assembly.

for power supply and voltage drop measurement were soldered with a low temperature solder (the melting point of 180 °C) to the side surfaces at the opposite ends. In order to secure the Ohmic contact between the test chip and the copper wire, a special solder with the melting point of 300 °C was applied to the chip with ultrasonic bonding method before soldering the copper wires. The lead wires were coated with a layer of adiabatic adhesion for minimizing heat loss. For measuring chip temperature, two 0.12 mm dia. T-type thermal couples for the local wall temperature measurement were adhered under the test chip at the center and at about 1.5 mm from the downstream end. The purpose of putting the 2nd thermocouple located at ~1.5 mm from the downstream end is to see the nonuniformity of wall temperature distribution. Generally, the measured wall temperature at the center of the chip was higher than that near the edge. The difference increased with increasing heat flux, reaching 8.5 K at the highest heat flux of about 145 W/cm^2. The heater temperature was obtained from the measured temperature at the center of chip on the bottom surface making a small correction (less than 1 K) for wall conduction. A uniform heat generation in the chip and adiabatic condition at the bottom surface was assumed in the calculation. A data acquisition unit was connected to a personal computer that automatically converted the thermocouples' output voltages into temperatures. Then the voltage drops of the test chip and the standard resistor were read and recorded eight times, and the average values of these measurements were adopted as experimental data.

The test channel on the bottom of which the test chip was fixed was made by Pyrex glass for visualizing flow boiling phenomena by use of a high speed video. To prevent the liquid from leaking out, the upper and nether covers were fastened by bolts and were seal with an O-ring. The local temperature of the test liquid at the chip level was measured by a T-type thermocouple the hot junction of which was located on a vertical line 25 mm apart from the edge of the test chip. The measured temperature was used as the bulk temperature of test fluid, T_b.

FC-72 was used as the working fluid with saturation temperature of 56 °C at atmospheric pressure. Experiments were performed for three fluid velocities (0.5, 1 and 2 m/s) and three liquid subcoolings (15, 25 and 35 K). The pressure at the inlet of the channel was kept at 1 atm. For the enhancement of boiling heat transfer, micro-pin-fins with square cross-sections were fabricated on the surface of silicon chip by use of the dry etching technique. To study the effects of height of micro-pin-fin, the micro-pin-finned chips having the same fin thickness of $t = 50$ μm and different fin heights of $h = 60$ (chip PF50-60), 120 μm (chip PF50-120) respectively, were tested. The fin pitch p was twice the



(a) Chip PF50-60 (b) Chip PF50-120

(a) (b)

Fig. 3. SEM images of micro-pin-fins.

Table 1
Experimental conditions.

Test surfaces	Liquid subcoolings (K)	Fluid velocities (m/s)	Inlet pressure (atm)
Chip PF50-120; Chip PF50-60; Chip S	15, 25, 35	0.5, 1.0, 2.0	1.0

fin thickness. The experimental conditions were listed in Table 1. The scanning-electron-micrograph (SEM) images of chips PF50-60 and PF50-120 are shown in Fig. 3(a) and (b), respectively. A smooth chip was also tested for comparison.

After FC-72 was infused, a frequency converter was adjusted to make the pump work at a required fixed mass flow rate. Then a cooling unit was run to control the liquid temperature in channels. When the loop reached steady state, the power supply was initiated to heat the test chip. A short-lived delay was imposed before initiating data acquisition to make sure that the steady-state conditions was attained. Power input to the test chip was increased in small steps up to the high heat flux region of nucleate boiling. The heat flux q was obtained from the voltage drop of the test chip and the electric current. An overheating protection system was incorporated in the power circuit. If the wall temperature sharply increases by more than 20 K in a short time, the data acquisition algorithm assumed the occurrence of CHF condition and the power supply was immediately shut down. The CHF value was computed as the steady state heat flux value just prior to the shutdown of the power supply.

A single sample was used for the micro-pin-finned chip, and two samples were used for the smooth surface. The experiment was repeated three times for each heater surface. The time interval between the subsequent runs was greater than 1 h. The boiling curves showed a good repeatability for all cases except for the boiling incipience point. Thus only the results for the third runs were presented in the paper. For characterizing surface-to-surface repeatability, we also tested two test chips of chip PF50-60. The boiling curves showed a good repeatability with a small heat flux deviation of less than 3% in the nucleate boiling region, which is in the range of uncertainty of 6% for the heat flux in the nucleate boiling region.

The uncertainties in the chip and bulk liquid temperature measurements by the thermocouples are estimated to be less than 0.3 K. Wall temperature uncertainty can be attributed to the errors caused by thermocouple calibration by a platinum resistance thermometer (0.03 K), temperature correction for obtaining surface temperature from the measured value at the bottom of the chip (0.2 K), the temperature unsteadiness (0.1 K) and the thermocouple resolution (less than 0.1 K). The uncertainty of the bulk temperature was due to errors caused by thermocouple calibration by a platinum resistance thermometer (0.03 K), the temperature unsteadiness (0.2 K) and the thermocouple resolution (less than 0.1 K). Heat flux uncertainty included the error of electric power supplied to the chip (0.11%), which was calculated from the errors of the current (0.014%) and voltage (0.1%) across the chip and heat loss by substrate heat conduction. The heat loss was estimated by solving three-dimensional conduction problems through substrate using a commercial software FLUENT with the measured wall temperature as a given condition, which was less than 16 and 6% for the forced convection and the nucleate boiling regions, respectively. It should be mentioned that q includes the heat transferred to the bulk liquid by conduction through the polycarbonate substrate.

3. Results and discussion

Fig. 4 shows the flow boiling curves of the smooth surface chip S. The single-phase, forced convection data clearly show the effects of fluid velocity. For comparison, the correlation of single-phase forced convection heat transfer proposed by Gersey and Mudawar [17] at $V = 0.5$ m/s is also shown in Fig. 4. The measured heat flux in the non-boiling region is about 20% higher than the correlation mainly due to the heat loss caused by conduction through the copper lead wires and the glass substrate and some uncertainties of the correlation itself. For a given fluid subcooling, the nucleate boiling curves almost collapse to one line, indicating that the heat transfer performance is dominated by the nucleate boiling heat transfer. The critical heat flux increase as fluid velocity is increased. By plotting the boiling curves with ΔT_b, the effect of fluid subcooling on nucleate boiling heat transfer appears to be directly related to subcooling level. The critical heat flux also increases with increasing fluid subcooling at a given fluid velocity. The pool boiling curve obtained from our previous work [9] for chip S at $\Delta T_{sub} = 25$ K is also shown in Fig. 4 for comparison. It can be seen that the smooth surface boiling curve is significantly shifted to the right compared to the flow boiling curve at $\Delta T_{sub} = 25$ K. This suggests that the boiling heat transfer performance is significantly affected by the fluid velocity in the low velocity range of 0 to 0.5 m/s. This phenomenon was also observed by Rainey et al. [16]. Using a highly polished thin gold film heater in R-113, Kirk et al. [18] found that increasing fluid velocity from 0.041 to 0.325 m/s significantly shifted the entire nucleate boiling curve to the left by about 5 K.

The flow boiling curves of chips PF50-60 and PF50-120 are shown in Figs. 5 and 6, respectively. The single-phase, forced convection curves for the micro-pin-finned surfaces show much higher heat flux than those for the smooth surface as shown in Fig. 4, in-

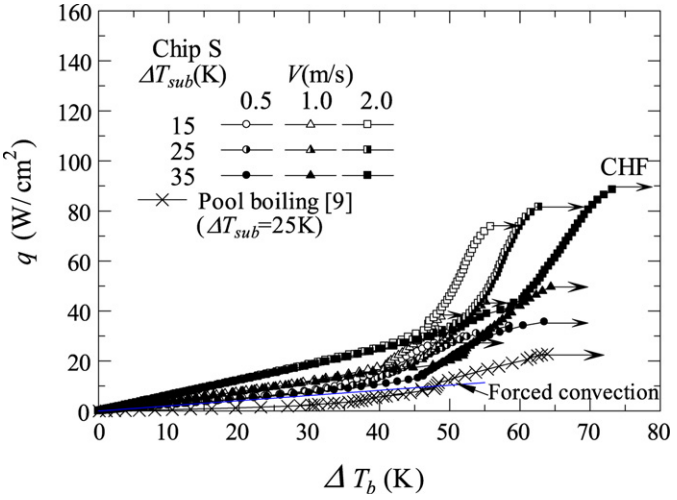


Fig. 4. Flow boiling curves of chip S.

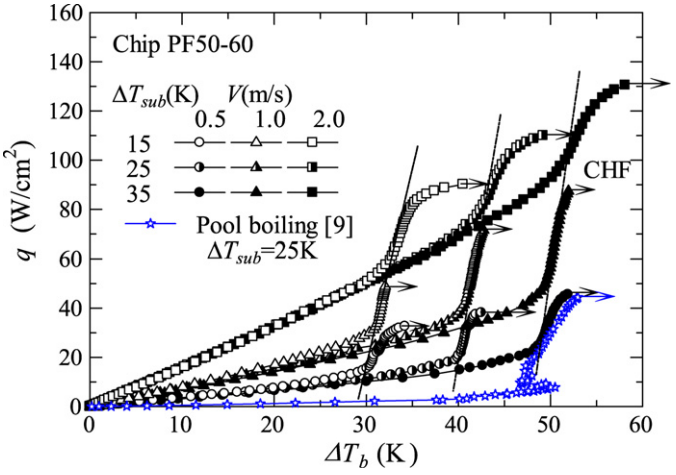


Fig. 5. Flow boiling curves of chip PF30-60.

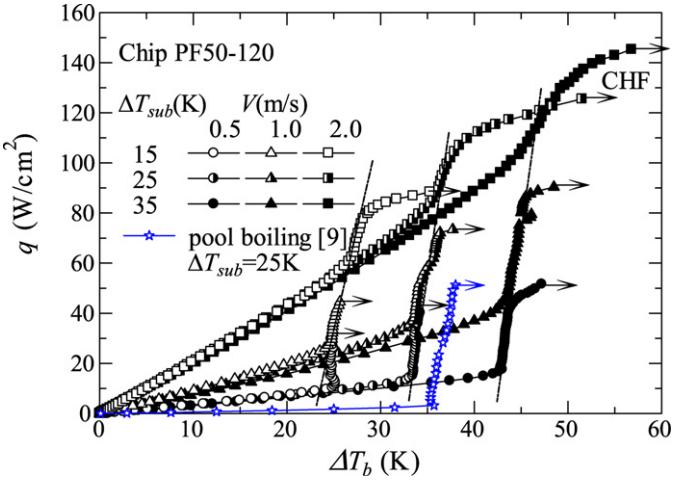


Fig. 6. Flow boiling curves of chip PF30-120.

dicating that the side walls of the micro-pin-fins are exposed to the fluid flow and are active for the forced convection heat transfer. This differs from the natural convection heat transfer in the pool boiling data of Wei and Honda [10], where the natural convection curves are not affected by the micro-pin-fins since they are completely submerged in the thermal boundary layer of superheated liquid. The single-phase convective heat transfer for chip PF50-120 is better than that of chip PF50-60 due to the larger heat transfer surface area. For a flow boiling case, the heat transfer process is dominated by the forced convection heat transfer and/or the nucleate boiling heat transfer. In the nucleate boiling region, we can see that all the flow boiling curves almost follow one line for a given liquid subcooling as indicated by the dashed line, showing insensitivity of the nucleate boiling heat transfer to fluid velocity. However, for the largest fluid velocity of 2 m/s and liquid subcooling of 35 K, the slope of the boiling curve becomes smaller, showing some effects of the forced convection heat transfer. For this case, the bubble size becomes much smaller through condensation, and is swept away immediately after its emission, leaving a large heater surface for single-phase, forced convection heat transfer. In addition, for the micro-pin-finned surface, when the fluid velocity is very large, the bubble nucleation on the bottom and side wall surfaces of the micro-pin-fin is easily affected by the forced flow over the chip surface, which prevents the burst of nucleate bubbles and thus reduces the proportion of nucleate boiling heat transfer. Since the heat transfer coefficient of a single-phase flow is smaller than that of a phase-change process, the large proportion of forced convection heat transfer makes the slope of the boiling curve become smaller. For comparison, the pool boiling curves of chips PF50-60 and PF50-120 at $\Delta T_{sub} = 25$ K obtained from our previous work [9] are also shown in Figs. 5 and 6, respectively. The large deviation of the pool boiling curve from the flow boiling curves at $\Delta T_{sub} = 25$ K suggests the fluid velocity has an obvious effect in the range of 0 to 0.5 m/s. This is probably due to the effect of bulk flow on the nucleation of the fin side wall and bubble motion in the fin gap. This phenomenon is different from the Rainey's porous surface [16], the fully developed boiling curves of which match together for the flow and pool boiling processes. Comparison of the CHF value of flow boiling and pool boiling, we found that the CHF value for chips PF50-60 and PF50-120 in pool boiling condition are greater than those in flow boiling condition at the fluid velocity of 0.5 m/s under the same liquid subcooling of 25 K. For low fluid velocities, the bubbles generated on the chip surface cannot be quickly swept away by the fluid flow, and the bubbles are easy to merge to form large ones. Since the channel height is only 5 mm, the large mushroom cannot detached from the surface easily due to the restriction of the upper channel wall, and the fresh bulk liquid cannot access the surface under the mushroom and thus it is easy to get an earlier burn out at high heat flux than the pool boiling for which the boiling space is large enough. This is not applicable to the smooth surface since the heat flux is not so high with smaller bubble size.

Figs. 7–9 show the comparison of boiling curves for all surfaces with $\Delta T_{sub} = 15$, 25 and 35 K, respectively. It can be seen that the slope of boiling curves increase in the order of chip S, PF50-60, PF50-120 for the same velocity, which shows that all micro-pin-fined surfaces have considerable heat transfer enhancement compared to a smooth surface. The enhancement of the heat transfer is considered as the surface area increase of the micro-pin-finned chip over a smooth surface, and the surface area enhancement of micro-pin-finned chip is further increased by changing the height of micro-pin-fins. The growth and movement of the bubbles within the confined gaps between fins can cause the micro-convection and form thin liquid layer for evaporation, which makes the profile of fins become effective heat transfer area, resulting in heat transfer enhancement. Observation of boiling phenomena on the micro-pin-finned chip revealed that this surface can cause more active nucleation sites, and makes the bubbles rest on surface for a longer time for evaporation, and thus increases the heat transfer performance. The wall superheats decrease in the order of chips S, PF50-60, PF50-120, and the wall temperature at the CHF point is

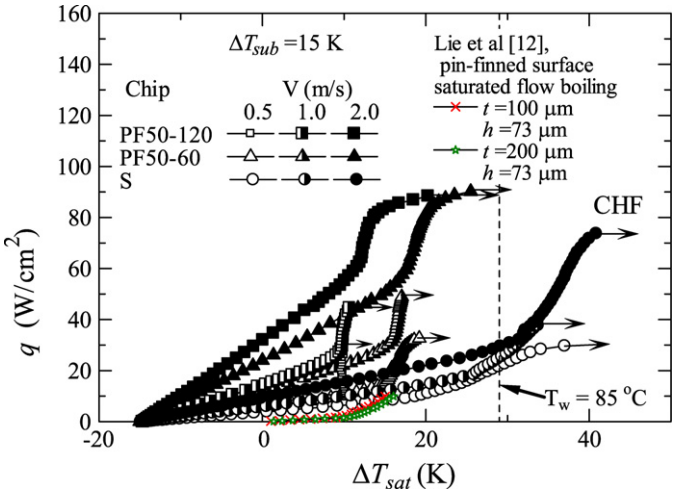


Fig. 7. Comparison of boiling curves for all chips at $\Delta T_{sub} = 15$ K.

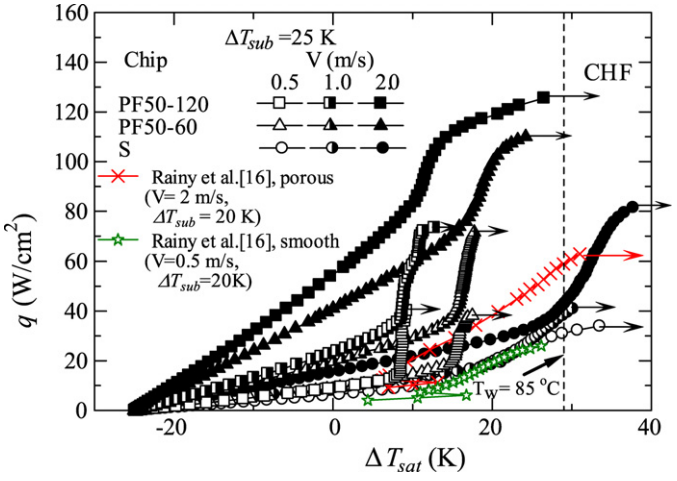


Fig. 8. Comparison of boiling curves for all chips at $\Delta T_{sub} = 25$ K.

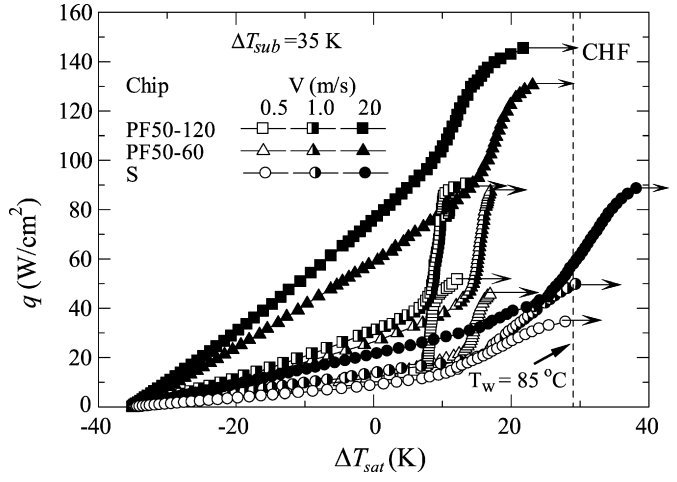


Fig. 9. Comparison of boiling curves for all chips at $\Delta T_{sub} = 35$ K.

less than the upper limit for the reliable operation of LSI chips, 85 °C, showing that the heat transfer can be further enhanced by increasing fin height again. For comparison, Lie et al.'s saturated boiling curves for two pin-finned surfaces [12] is shown in Fig. 7 and Rainey et al.'s boiling curve with the liquid subcooling of 20 K for the smooth surface at 0.5 m/s and the microporous surface at

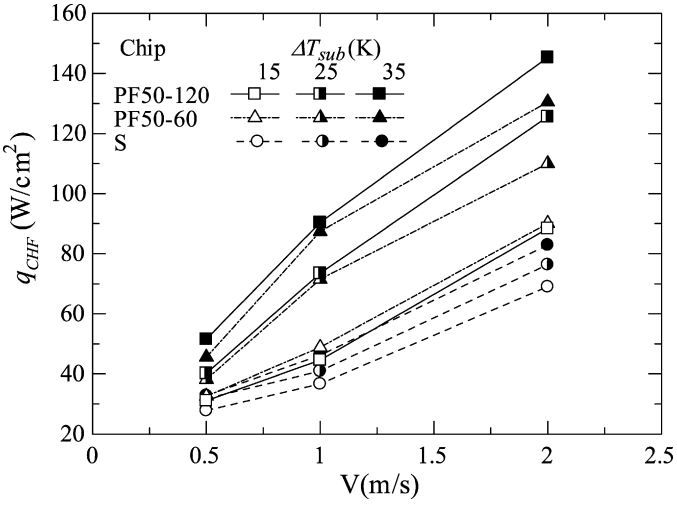


Fig. 10. Effect of fluid velocities and subcoolings on CHF.

2 m/s [16] is shown in Fig. 8. The boiling curve of the smooth surface of Rainey et al. agrees well with the present data except for a lower CHF value mainly due to the lower liquid subcooling. The single-phase, forced convection curve of the microporous surface is worse than the smooth surface, chip S, for the same velocity of 2 m/s, mainly due to the lower effective thermal conductivity of the microporous coating layer as explained by Rainey et al. [16]. Although having an earlier boiling incipience, the microporous surface shows a larger wall superheat than the micro-pin-finned surfaces in the nucleate boiling region, and the heat flux at 85 °C is less than half the CHF of chip PF50-120. The boiling curves of Lie et al.'s pin-finned surface with the larger fin thicknesses of 100 and 200 μm [12] show a much smaller slope and a larger wall superheat compared to that of the present micro-pin-finned surfaces. The wall superheat decreases in the order of 200, 100 and 50-μm micro-pin-fins. In the previous pool boiling study, we have found that the boiling heat transfer performance for the micro-pin-finned surface with the fin thickness of 10–50 μm is much better than the pin-finned surface with the larger fin thickness of about 300 μm used by Anderson and Mudawar [2], and the fin thickness of 30–50 μm is a suitable range for effectively enhancing boiling heat transfer. The optimum fin size is considered to be determined by the balance of the capillary force for driving the micro-flow in the gap of micro-pin-fins and the flow resistance. The present flow boiling study again shows the larger fin thickness above 100 μm is not so remarkably effective compared to the fin thickness of 50 μm. Careful comparison of flow boiling curves for different liquid subcoolings of 15, 25 and 35 shows that the boiling curves in the nucleate region are almost not affected by liquid subcooling, again indicating that the nucleate boiling dominates the heat transfer process.

Fig. 10 shows the CHF versus fluid velocity for chips S, PF50-60 and PF50-120 with fluid subcooling as a parameter. The fluid velocity has a very large effect on CHF. For the low fluid subcooling of 15 K and the velocity larger than 1 m/s, the rate of CHF enhancement is increased remarkably, which was also supported by many researchers such as Mudawar and Maddox [13], Rainey and You [16], etc., who had noted that the transition from low to high velocity was characterized by an increase in the rate of CHF enhancement with velocity. However, for the large liquid subcoolings of 25 and 35 K, there is no such obvious transition. For a low fluid subcooling, as explained by Mudawar and Maddox [13], the low velocity CHF was caused by dryout of the liquid sublayer beneath a large continuous vapor blanket near the downstream edge of the heater; however in the high velocity CHF regime, the thin vapor layer covering the surface was bro-

ken into continuous vapor blankets much smaller than the heater surface, decreasing the resistance of fluid flow to rewet the liquid sublayer and thus providing an additional enhancement to CHF and subsequent increase in slope. For a large fluid subcooling, the bubble size becomes small and the heater surface was not fully occupied with vapor layer for the fluid velocity range in this study. In addition, for the micro-pin-finned surface, when the fluid velocity is very large, the bubble nucleation on the bottom and side wall surfaces of the micro-pin-fin is easily affected by the forced flow over the chip surface. Therefore, the forced convection heat transfer takes a large proportion, and the slope becomes smaller after 1 m/s as seen in Fig. 10. The enhancement of CHF by the fluid velocity and subcooling for micro-pin-fined surfaces is more noticeable compared to a smooth surface. For chip PF50-120, the CHF reaches nearly 145 W/cm^2 at 2 m/s and 35 K.

4. Conclusions

The present study investigates the effects of fluid velocity, subcooling and fin height on the flow boiling heat transfer performance of FC-72 from simulated silicon chips. The data are also compared with the smooth surface and the previous published pool boiling data. The main conclusions can be summarized as follows:

1. The flow boiling curves for the micro-pin-finned surfaces in the nucleate boiling region are almost not affected by the fluid velocity and subcooling in the present investigated range, but shift towards a smaller wall temperature compared to that of the pool boiling case, showing some effects of fluid velocity in the range of 0–0.5 m/s.
2. All micro-pin-fined surfaces have considerable heat transfer enhancement compared to a smooth surface, and the slope of boiling curves increases in the order of chips S, PF50-60 and PF50-120 for the same fluid velocity and subcooling.
3. The CHF values for all surfaces increase with fluid velocity and subcooling, and the enhancement of CHF for the micro-pin-finned surfaces is more noticeable than smooth chip.
4. For a lower liquid subcooling of 15 K, the rate of CHF enhancement is increased remarkably above the fluid velocity of 1 m/s; however for a larger liquid subcooling of 35 K, the rate of CHF enhancement is decreased above 1 m/s. This is due to the increased effect of single-phase forced convection heat transfer with increasing liquid subcooling and fluid velocity.
5. The maximum CHF of 145 W/cm^2 is obtained by chip PF50-120 at 2 m/s and 35 K, and the wall temperature for the micro-pin-finned surfaces is less than the upper temperature limit for the normal operation of LSI chip, 85 °C.

Acknowledgements

This work is supported by the National Fundamental Research Program of China (No. 2006CB601203), the key project of State Education Ministry of China (No. 106142) and the program for new century excellent talents in university (NCET-07-0680).

References

[1] S. Oktay, Departure from natural convection (DNC) in low-temperature boiling heat transfer encounted in cooling micro-electronic LSI devices, in: Proceeding of 7th International Heat Transfer Conference, Munich, vol. 4, 1982, pp. 113–118.
[2] T.M. Anderson, I. Mudawar, Microelectronic cooling by enhanced pool boiling of a dielectric fluorocarbon liquid, ASME J. Heat Transfer 111 (1989) 752–759.
[3] U.P. Hwang, K.F. Moran, Boiling heat transfer of silicon integrated circuits chip mounted on a substrate, Heat Transfer Electron. Equip. ASME HTD 20 (1981) 53–59.
[4] N.K. Phadke, S.H. Bhavnani, A. Goyal, R.C. Jaeger, J.S. Goodling, Re-entrant cavity surface enhancements for immersion cooling of silicon multichip packages, IEEE Trans. Comp. Hybrids Manufact. Technol. 15 (1992) 815–822.
[5] H. Kubo, H. Takamatsu, H. Honda, Effects of size and number density of micro-reentrant cavities on boiling heat transfer from a silicon chip immersed in degassed and gas dissolved FC-72, J. Enhanced Heat Transfer 6 (1999) 151–160.
[6] J.P. O'Connor, S.M. You, D.C. Price, A dielectric surface coating technique to enhance boiling heat transfer from high power microelectronics, IEEE Trans. Comp. Packaging Manufact. Technol. 18 (1995) 656–663.
[7] K.N. Rainey, S.M. You, S. Lee, Effect of pressure, subcooling, and dissolved gas on pool boiling heat transfer from microporous, square pin-finned surfaces in FC-72, Int. J. Heat Mass Transfer 46 (2003) 23–25.
[8] H. Honda, H. Takamastu, J.J. Wei, Enhanced boiling of FC-72 on silicon chips with micro-pin-fins and submicron-scale roughness, Journal of Heat Transfer 124 (2002) 383–390.
[9] J.J. Wei, Experimental study on enhanced boiling heat transfer from silicon chips with micro-pin-fins and submicro-roughness, PhD dissertation, Kyushu University, 2002.
[10] H. Honda, J.J. Wei, Enhanced boiling heat transfer from electronic components by use of surface microstructures, Experimental Thermal and Fluid Science 28 (2004) 159–169.
[11] J.J. Wei, L.J. Guo, H. Honda, Experimental study of boiling phenomena and heat transfer performances of FC-72 over micro-pin-finned silicon chips, Heat and Mass Transfer 41 (2005) 744–755.
[12] Y.M. Lie, J.H. Ke, W.R. Chang, T.C. Cheng, T.F. Lin, Saturated flow boiling heat transfer and associated bubble characteristics of FC-72 on a heated micro-in-finned silicon chip, Int. J. Heat Mass Transfer 50 (2007) 3862–3876.
[13] I. Mudawar, D.E. Maddox, Critical heat flux in subcooled flow boiling of fluorocarbon liquid on a simulated electronic chip in a vertical rectangular channel, Int. J. Heat Mass Transfer 32 (1989) 379–394.
[14] S.S. Kutateladze, B.A. Burakov, The critical heat flux for natural convection and forced flow of boiling and subcooled dowtherm, in: Problems of Heat Transfer and Hydraulics of Two-Phase Media, Pergamon, Oxford, 1989, pp. 63–70.
[15] K.R. Samant, T.W. Simon, Heat transfer from a small heated region to R-113 and FC-72, ASME J. Heat Transfer 111 (1989) 1053–1059.
[16] K.N. Rainey, G. Li, S.M. You, Flow boiling heat transfer from plain and microporous coated surfaces in subcooled FC-72, ASME J. Heat Transfer 123 (5) (2001) 918–925.
[17] C.O. Gersey, I. Mudawar, Effects of orientation on critical heat flux from chip arrays during flow boiling, Trans. ASME J. Electr. Pack. 114 (1992) 290–299.
[18] K.M. Kirk Jr., H. Merte, R. Keller, Low-velocity subcooled nucleate flow boiling at various orientations, ASME J. Heat Transfer 117 (1995) 380–386.